

PCN Number:	20180118002	PCN Date:	January 19, 2018
Title:	Datasheet for DRV8320, DRV8320R, DRV8323, DRV8323R		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



DRV8320, DRV8320R
DRV8323, DRV8323R

SLVSDJ3B – FEBRUARY 2017 – REVISED DECEMBER 2017

Changes from Revision A (April 2017) to Revision B	Page
• Changed the low-power sleep mode supply current from the maximum value (20 μ A) to the typical value (12 μ A) in the <i>Features</i>	1
• Changed the <i>Applications</i>	1
• Changed the GAIN value from 45 k Ω to 47 k Ω in the test condition of the amplifier gain for the H/W device in the <i>Electrical Characteristics</i> table	14
• Deleted t_{EN_NCS} from the <i>SPI Slave Mode Timing Diagram</i>	17
• Added a note to the <i>Synchronous 1x PWM Mode</i> to define <i>!PWM</i>	30
• Updated the <i>Auto Offset Calibration</i> section	43
• Updated the <i>V_{DS} Latched Shutdown</i> and <i>V_{DS} Automatic Retry</i> sections	47
• Updated the <i>Sleep Mode</i> section	49
• Changed the address listed in the title for the <i>Gate Drive LS Register</i> section to the correct register address, 0x04	57
• Changed the maximum Q_g value for both trapezoidal and sinusoidal commutation the $V_{VM} = 8$ V example of the <i>Detailed Design Procedure</i>	62
• Changed I_{DRIVEP} and I_{DRIVEN} equations in the <i>IDRIVE Configuration</i> section	63

The datasheet number will be changing.

Device Family	Change From:	Change To:
DRV8320, DRV8320R, DRV8323, DRV8323R	SLVSDJ3A	SLVSDJ3B

These changes may be reviewed at the datasheet links provided.
<http://www.ti.com/product/DRV8320>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DRV8320HRTVR	DRV8320RSRHAR	DRV8323HRTAR	DRV8323RSRGZR
DRV8320HRTVT	DRV8320RSRHAT	DRV8323HRTAT	DRV8323RSRGZT
DRV8320RHRHAR	DRV8320SRTVR	DRV8323RHRGZR	DRV8323SRTAR
DRV8320RHRHAT	DRV8320SRTVT	DRV8323RHRGZT	DRV8323SRTAT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
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