AOV11S60

600V 8A αMOS™ Power Transistor

General Description

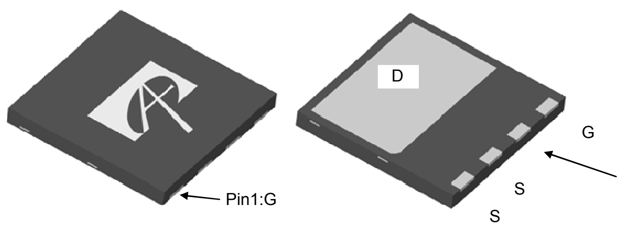
The AOV11S60 has been fabricated using the advanced αMOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications.
By providing low $R_{DS(on)}$, Q_g and E_{OSS} along with guaranteed avalanche capability this part can be adopted quickly into new and existing offline power supply designs.

Product Summary

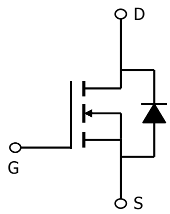
V_{DS} @ $T_{j,max}$	700V
I_{DM}	45A
$R_{DS(ON),max}$	0.5Ω
$Q_{g,typ}$	11nC
E_{oss} @ 400V	2.7µJ

100% UIS Tested
100% R_g Tested

DFN8X8



AOV11S60



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C=25°C	I_D	8	A
	T_C=100°C		7.0	
Pulsed Drain Current [C]		I_{DM}	45	
Continuous Drain Current	T_A=25°C	I_{DSM}	0.65	A
	T_A=70°C		0.22	
Avalanche Current [C]		I_{AR}	2	A
Repetitive avalanche energy [C]		E_{AR}	60	mJ
Single pulsed avalanche energy [G]		E_{AS}	120	mJ
Power Dissipation [B]	T_C=25°C	P_D	156	W
	Derate above 25°C		1.25	W/ °C
Power Dissipation [A]	T_A=25°C	P_{DSM}	8.3	W
	T_A=70°C		5.3	
MOSFET dv/dt ruggedness		dv/dt	100	V/ns
Peak diode recovery dv/dt [H]			20	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds [J]		T_L	300	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	12	15	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.6	0.8	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V, T_J=25°C	600	-	-	V
		I_D=250µA, V_{GS}=0V, T_J=150°C	650	700	-	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=600V, V_{GS}=0V	-	-	1	µA
		V_{DS}=480V, T_J=150°C	-	10	-	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=5V, I_D=250µA	2.8	3.5	4.1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=3.8A, T_J=25°C	-	0.42	0.5	Ω
		V_{GS}=10V, I_D=3.8A, T_J=150°C	-	1.17	1.4	Ω
V_{SD}	Diode Forward Voltage	I_S=5.5A, V_{GS}=0V, T_J=25°C	-	0.84	-	V
I_S	Maximum Body-Diode Continuous Current		-	-	8	A
I_{SM}	Maximum Body-Diode Pulsed Current[C]		-	-	45	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz	-	545	-	pF
C_{oss}	Output Capacitance		-	37.3	-	pF
$C_{o(er)}$	Effective output capacitance, energy related[H]	V_{GS}=0V, V_{DS}=0 to 480V, f=1MHz	-	30.8	-	pF
$C_{o(tr)}$	Effective output capacitance, time related[I]		-	93.6	-	pF
C_{rss}	Reverse Transfer Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz	-	1.42	-	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	16.5	-	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=480V, I_D=5.5A	-	11	-	nC
Q_{gs}	Gate Source Charge		-	2.8	-	nC
Q_{gd}	Gate Drain Charge		-	3.8	-	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=400V, I_D=5.5A, R_G=25Ω	-	20	-	ns
t_r	Turn-On Rise Time		-	20	-	ns
$t_{D(off)}$	Turn-Off DelayTime		-	59	-	ns
t_f	Turn-Off Fall Time		-	20	-	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=5.5A, dI/dt=100A/µs, V_{DS}=400V	-	250	-	ns
I_{rm}	Peak Reverse Recovery Current	I_F=5.5A, dI/dt=100A/µs, V_{DS}=400V	-	21	-	A
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=5.5A, dI/dt=100A/µs, V_{DS}=400V	-	3.3	-	µC

A. The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A=25°C.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C, Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
G. L=60mH, I_{AS}=2A, V_{DD}=150V, Starting T_J=25°C
H. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$.
I. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$.
J. Wavesoldering only allowed at leads.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

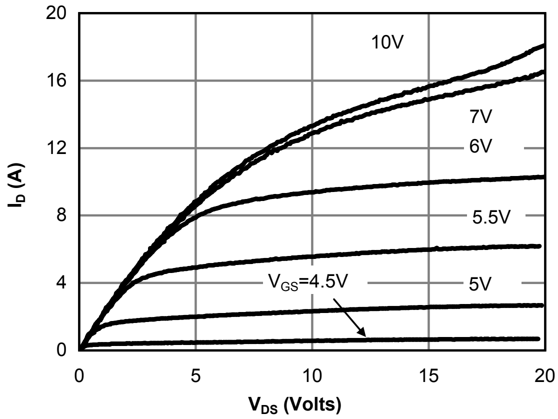


Figure 1: On-Region Characteristics@25°C

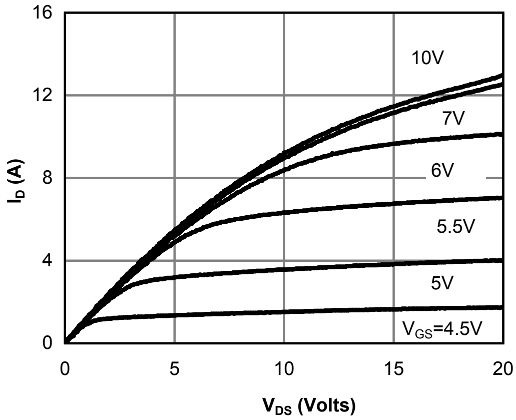


Figure 2: On-Region Characteristics@125°C

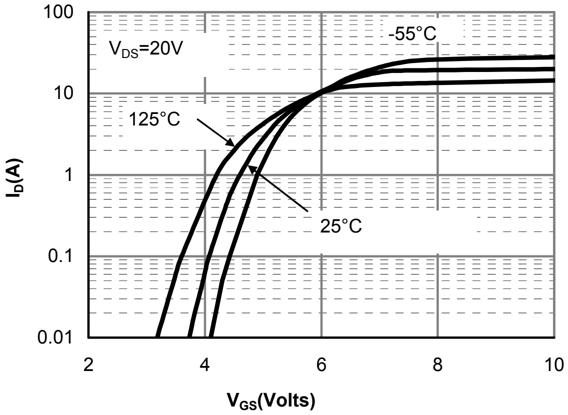


Figure 3: Transfer Characteristics

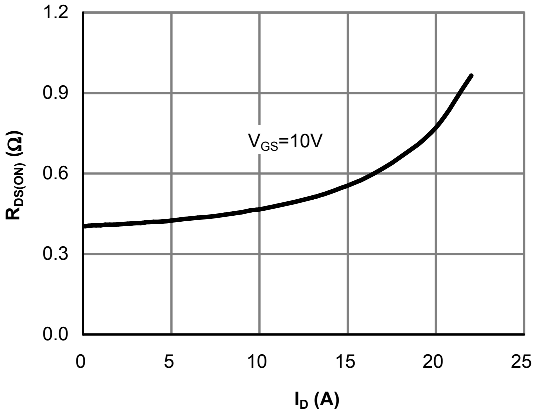


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

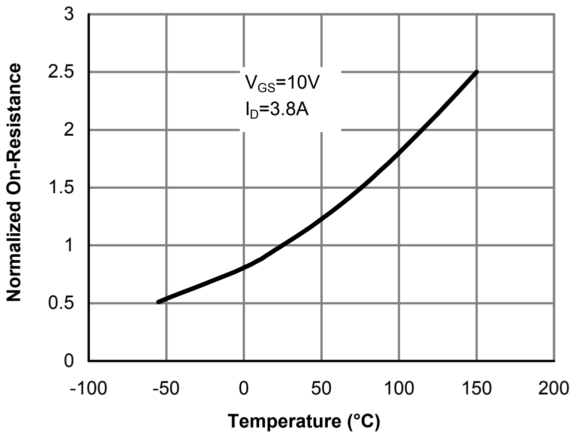


Figure 5: On-Resistance vs. Junction Temperature

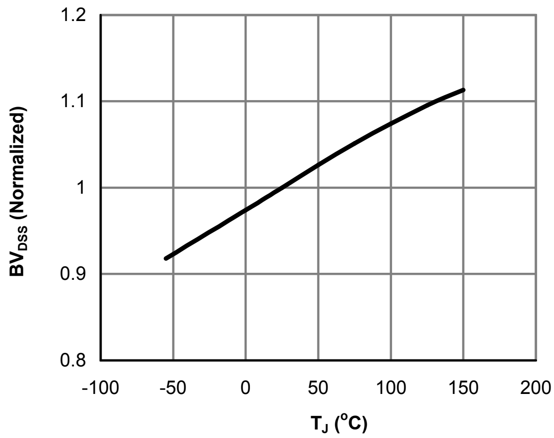


Figure 6: Break Down vs. Junction Temperature

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

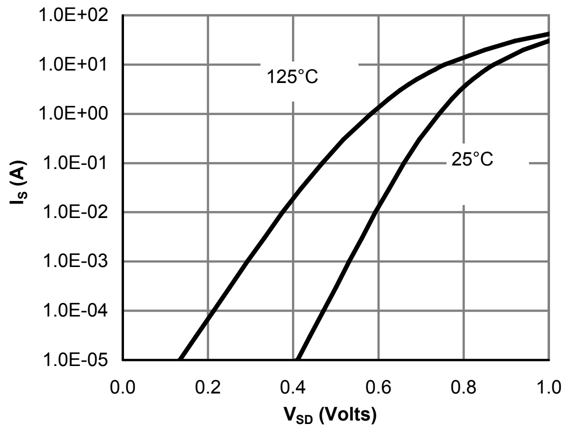


Figure 7: Body-Diode Characteristics (Note E)

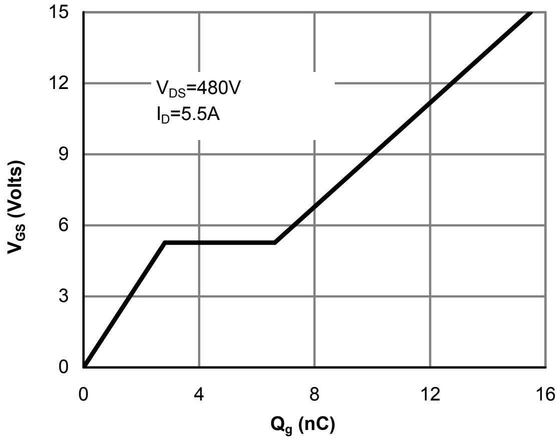


Figure 8: Gate-Charge Characteristics

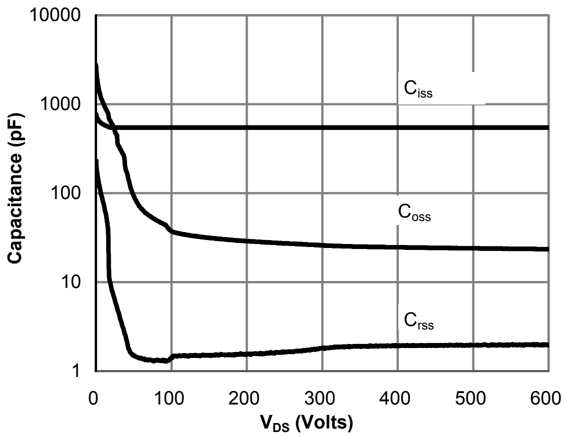


Figure 9: Capacitance Characteristics

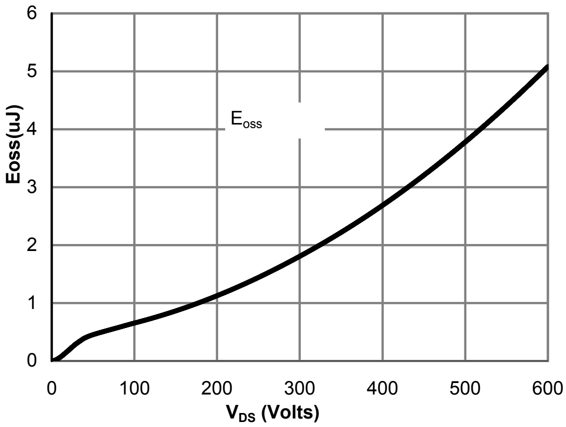


Figure 10: Coss stored Energy

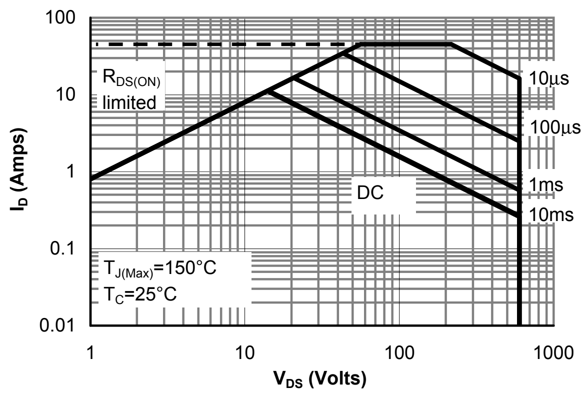


Figure 11: Maximum Forward Biased Safe Operating Area for AOT(B)11S60 (Note F)

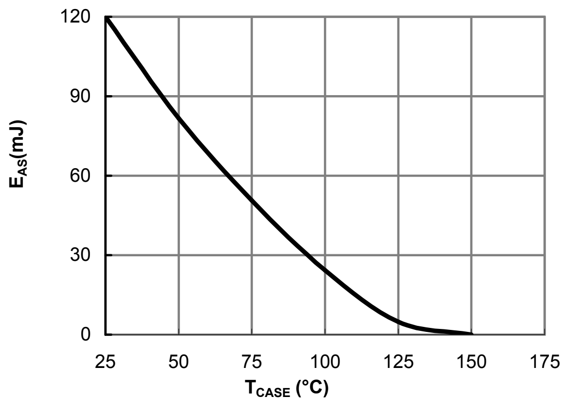


Figure 12: Avalanche energy

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

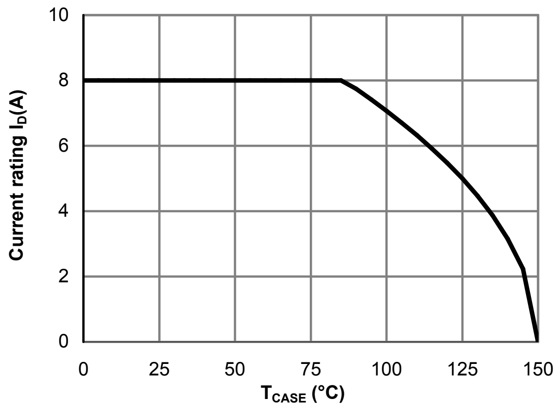


Figure 14: Current De-rating (Note B)

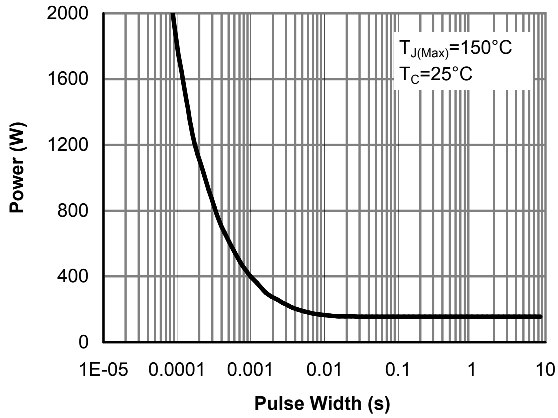


Figure 14: Single Pulse Power Rating Junction-to-Case (Note F)

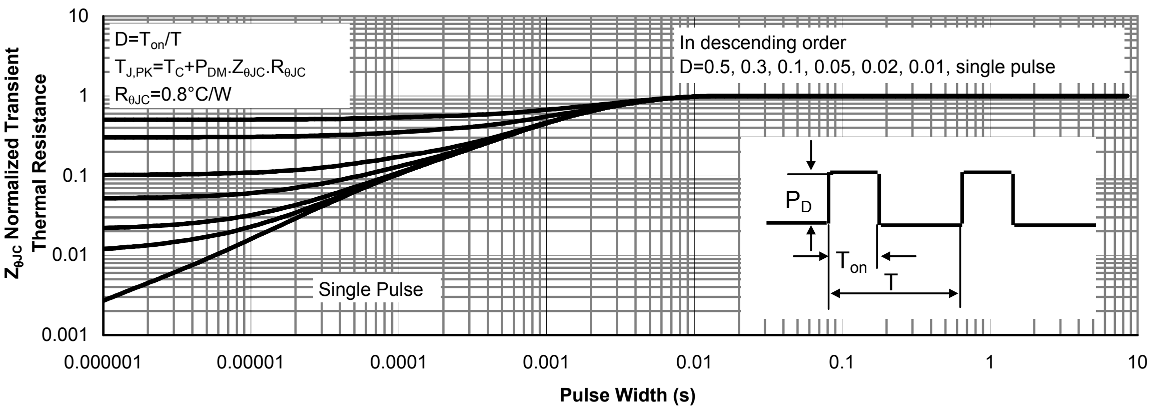


Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

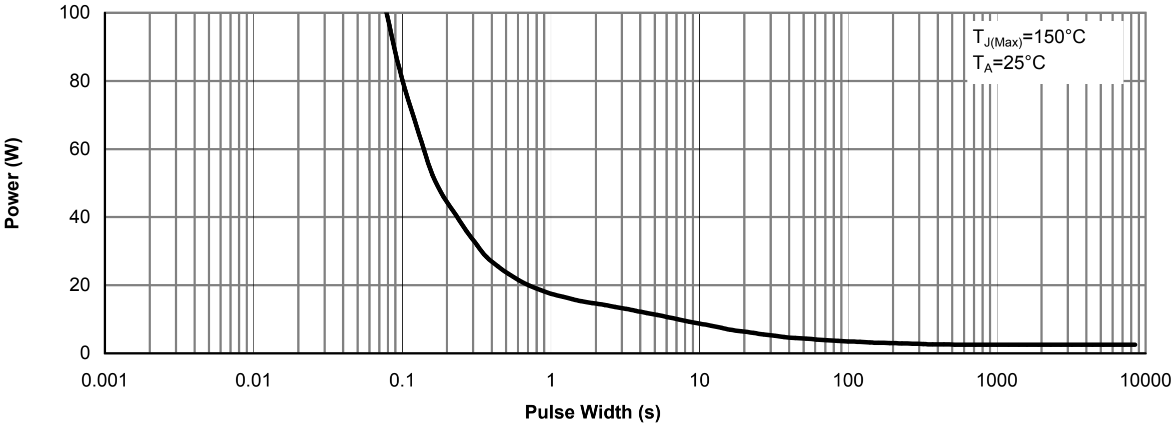


Figure 16: Single Pulse Power Rating Junction-to-Ambient (Note G)

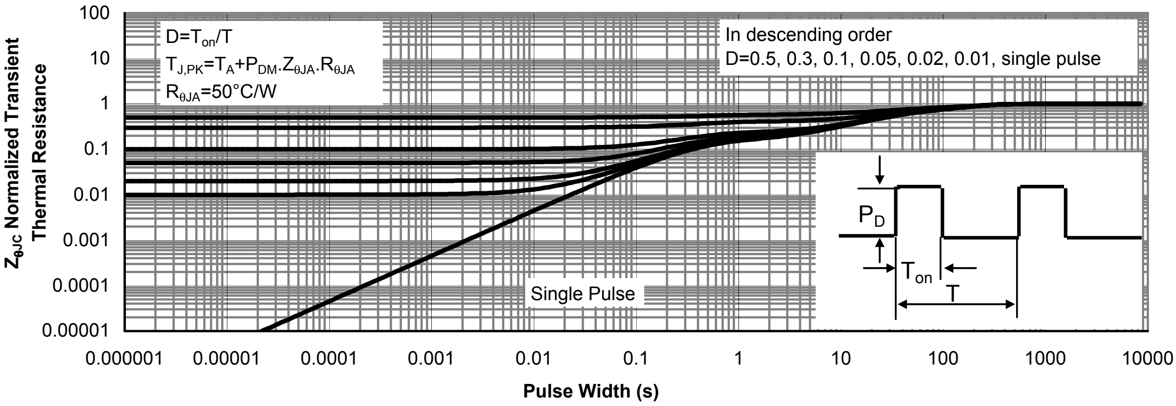
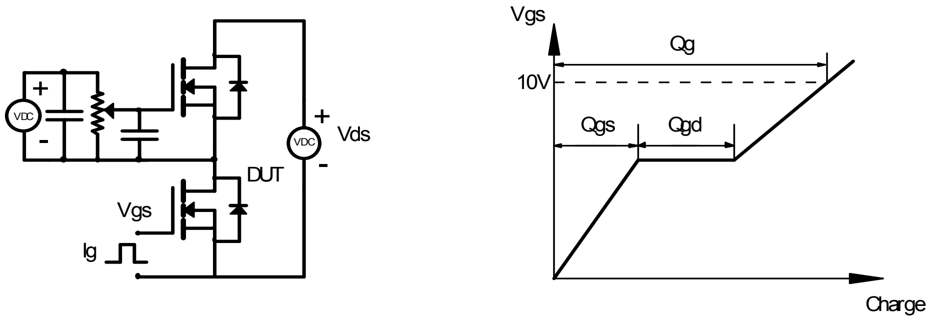
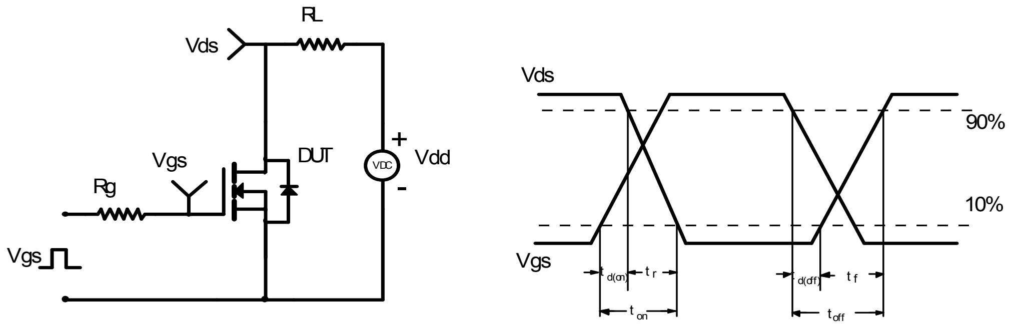


Figure 17: Normalized Maximum Transient Thermal Impedance (Note G)

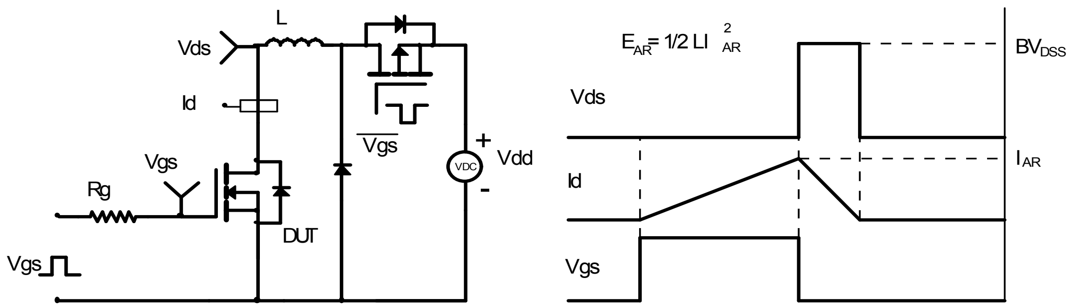
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms